IV. Remarks:

Reconsideration of this application in light of the above amendments and the following remarks is requested. Claims 1 and 32-56 were previously pending in this application. Claim 1 has been cancelled. Claim 38, 46, and 55 have been amended. Claims 32-37, 39-45, 47-54, and 56 have been maintained in their previous form. Claims 57-62 have been added. Claims 32-62 are currently pending.

Election/Restrictions

Claim 1 has been cancelled.

Specification

As suggested, the title has been changed to:

A Self-Passivated Copper Interconnect Structure

Claim Rejections – 35 USC § 103

Rejection of Claims 32, 33, 37-39, 41, 45-47, 49, 50, and 54-56

Claims 32, 33, 35, 40, 41, 43, 48, 49, 50, and 52 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over US patent 6,387,805 to Ding et al. (hereinafter "Ding") in view of the article titled "Titanium-nitride self encapsulation of Cu and Ag films on silicon oxide" by Adams et al.(hereinafter "Adams"). The applicant respectfully traverses the rejection as follows.

As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness, ... the prior art reference (or references when combined) must teach or suggest all the claim limitations." As discussed below, this prima facie case of obviousness is not met in the pending claims.

Ding described that "the alloying element diffuses towards the dielectric layer 54 and forms a very thin barrier layer 64, as illustrated in the enlarged cross-sectional view in FIG. 4, at the interface between the seed layer 60 and the dielectric layer 54 that prevents copper from diffusing into and through the silica dielectric layer 54. The barrier layer 64 comprises an oxide of the alloying element along with some of the silicon." (column 6, lines 25 to 31). Claim 1 of Ding's also describes "a first step of sputter depositing onto a dielectric part of a substrate comprising silicon and oxygen[,] a copper alloy layer." Ding thus teaches a barrier layer between the seed layer and the dielectric layer, wherein the barrier layer comprises an oxide of the alloying element along with silicon, and the dielectric layer comprises silicon and oxygen.

Claim 32 in the present disclosure describes "an insulating layer over a semiconductor structure having an opening therein; a fill layer comprised of Cu and Ti filling said opening in said insulating layer; and a self-passivation layer comprised of titanium nitride over said fill layer." The present disclosure provides a self-passivation layer disposed *over* the copper titanium alloy layer, wherein the self-passivation layer comprises titanium nitride and the insulating layer does not necessarily have silicon and oxygen. Ding teaches away from the present disclosure and can not be used for the rejection.

This difference is not alleviated by Adams. Adams describes "alloy films consisting of ~200 nm Cu (27 at. % Ti), and Ag (6-26 at. % Ti)" (the first line of Section 2. Experimental in page 449) wherein the copper alloy layer comprises 27 at. % Ti. Ding teaches that "a first step of sputter depositing onto a dielectric part of a substrate comprising silicon and oxygen a copper alloy layer comprising copper and less than 10 atomic percent of an alloying element; and a second step of depositing onto said copper alloy layer a copper layer" (Claim 1) wherein the alloying element is less than 10 at. %".

Ding described that "the alloying element diffuses towards the dielectric layer 54 and forms a very thin barrier layer 64, as illustrated in the enlarged cross-sectional view in FIG. 4, at the interface between the seed layer 60 and the dielectric layer 54" (lines

25~28 in column 6) and "the annealing is preferably performed within the temperature range of 300 to 400 °C." (lines 39~40 in column 6). In contrast, Adams teaches that "the sample annealed at 450 ^{0}C differs from the as-deposited sample only by the presence of a thin surface oxide layer of ~10 nm. The increased surface Ti peak suggests that at this temperature Ti only segregates to the free surface, presumably to react with oxygen and nitrogen from the ambient. This outdiffusion of Ti makes the subsurface layer of the alloy Cu-rich. The samples annealed at 500 0C and 650 0C clearly show the appearance of two separate Ti signals, resulting from the segregation of Ti to the free surface and also to the alloy/SiO2 interface." (2nd paragraph of section 3. Results in page 449). Adams clearly suggests that the Ti oxide layer can be formed at the alloy/SiO2 interface only when the temperature is above 450 ^{0}C.

Thus, the two references teach away from each other and cannot be combined. Accordingly, the cited references cannot support the rejection.

Rejection of Claims 32, 33, 37-39, 41, 45-47, 49, 50, and 54-56

Claims 32, 33, 37-39, 41, 45-47, 49, 50, and 54-56 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over US patent 6,693,356 to Jiang et al. (hereinafter "Jiang") in view of Adams. The applicant respectfully traverses the rejection as follows.

Jiang, in claim 1, describes "an integrated circuit in the horizontal surface of a semiconductor body comprising a dielectric layer over said semiconductor body; a substantially vertical hole through said dielectric layer, said hole having sidewalls and a bottom; a barrier layer over said dielectric layer including said sidewalls within said hole and said bottom of said hole, said barrier layer operable to seal copper; a copper-doped transition layer with a gradient copper doping having a resistivity higher than pure copper over said barrier layer wherein said copper-doped transition layer is a material selected from the group consisting of copper titanium, copper magnesium, copper aluminum, copper silicon, copper chromium, copper beryllium, copper zirconium, copper nickel, copper zinc, copper silver, and copper tin; and the remainder of said hole filled with

copper". Jiang further teaches an integrated circuit comprising a copper-doped layer and the remainder of said hole filled with copper.

In contrast to the two-step fill procedure of Jiang, claim 32, describes "an insulating layer over a semiconductor structure having an opening therein; a fill layer comprised of Cu and Ti filling said opening in said insulating layer; and a self-layer comprised of titanium nitride over said fill layer." There is no additional copper layer filled in the opening.

Furthermore, according to Jiang, the copper-doped transition layer has "a gradient copper doping" (claim 1) and "preferred choices are copper zirconium and copper tin" (line 64 in column 4). The copper-doped transition layer is interposed between the barrier layer and the copper layer in the final structure (see above cited claim 1 of Jiang's). In claim 32 of the present disclosure, the fill layer comprises copper titanium and said Ti is essentially uniformly distributed through said fill layer as described in claims 40, 48, and 49. As such, Jiang teaches away from the present disclosure and can not be used for the rejection.

Therefore, the combination of the cited references fails to teach or suggest all claim limitations.

Furthermore, Adams teaches "silver- and copper-titanium alloys on silicon dioxide of decompositions varying from 4 to 27 at. % Ti" (in the Abstract) and "alloy films consisting of ~200 nm Cu (27 at. % Ti), and Ag (6-26 at.% Ti) were deposited by electron-beam evaporation onto thermally grown SiO2 (100-200 nm) on (100) Si substrate" (lines 1 to 4 of Section 2. Experimental in page 449). Copper-titanium alloy is directly deposited on SiO_2 layer such that a titanium oxide layer can be formed between the copper-titanium alloy layer and the silicon oxide layer. In Jiang's claim 1, "a copper-doped transition layer with a gradient copper doping having a resistivity higher than pure copper over said barrier layer" wherein the copper-doped transition layer is over the barrier layer instead of a silicon oxide layer. Jiang and Adams teach away from each other and can not be combined for the rejection.

As such, an unobvious difference between the claimed product and prior art product are set forth. Jiang and Adams, whether taken single or in combination, fail to teach each element of the claim 32, 41, or claim 49, and therefore, cannot support an anticipation rejection of claim 32, 41, and claim 49. Accordingly, the cited references cannot support an anticipation rejection of the dependent claims 33, 37-39, 45-47, 50, and 54-56 since claims 33, 37-39, 45-47, 50, and 54-56 depend from and further limit corresponding independent claim 32, 41, or 49.

Rejections of Claims 34, 36, 42, 44, 51, and 53

Claims 34, 36, 42, 44, 51, and 53 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over US patent 6,387,805 to Ding in view of "Titanium-nitride self encapsulation of Cu and Ag films on silicon oxide" by Adams as applied to claims 32, 41, and 49 above, and further in view of US patent 6,472,231 to Gabriel et al (hereinafter "Gabriel"). With respect to claims 34, 42, and 51 Ding and Admas fail to disclose the low-k dielectric insulation layer. However, Gabriel discloses the use of both the low-k dielectric insulation layers and a dual damascene structure (column 1 and column 3). The applicant respectfully traverses the rejection as follows.

As commented above, claims 32, 41, and 49 are now in condition for allowance. Claims 34, 36, 42, 44, 51, and 53 depend from and further limit the independent claims 32, 41, and 49, respectively, these claims are now in condition for allowance as well.

Furthermore, both Ding and Adams teach a copper alloy layer on a silicon oxide layer, in which the silicon oxide layer is not a low-k dielectric insulation material. Ding and Adams teach away from Gabriel's and can not be combined for the rejection.

D. Conclusion

Based on the foregoing, independent claims 32, 41, and 49 are now in condition for allowance. As dependent claims 33-40, 42-48, and 50-56 depend from and further limit the independent claims 32, 41, and 49, respectively, these claims are now in condition for allowance as well. Claims 38, 46, and 55 have been amended. Claims 57-62 have been added according to

specification. No new matter has been added. An early formal notice of allowance of claims is requested.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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Dated: 2-21-05

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